REMARKS

Reconsideration of this application is respectfully requested. Claims 28-35 and 62-67 remain pending. The remarks below in connection with claim rejections refer to the claims as amended herein.

Rejection Under 35 U.S.C. § 102(b)

Claims 28, 34-35 and 62 have been rejected as being anticipated by U.S. Patent Application No. 10/000,122 to Nataraj et al. (Nataraj). Applicant respectfully submits that claims 28, 34-35 and 62 are not anticipated by Nataraj.

Claim 28 recites, in part:

> a write mapping circuit to convert an input data word into a converted data word based on both data bits and mask bits within the input data word, the converted data word having one of at least two different patterns of constituent bits according to the state of a first control signal;

Nataraj describes a mask generating circuit within the selective coding logic 1219 to provide a mask word to the array read/write circuit 1215 in conjunction with Figure 12 (Nataraj, paragraph 161), and a plurality of decoder subcircuits (1623, 1625 and 1627) within the decoder circuit 1611 that receive and decode the prefix length value to generate a corresponding mask word in conjunction with Figure 16. (Nataraj, paragraph 193, lines 11-14). Assuming, arguendo, that either the selective coding logic 1219 of Figure 12, or the decoder circuit 1611 comprising decoder subcircuits 1623, 1625 and 1627 of Figure 16 correspond to the write mapping circuit of claim 28, as suggested in the Office Action, Nataraj describes a prefix length value that is encoded by the encoding circuits of Figures 12 and 16 into a mask word. However, Nataraj does not disclose or suggest a write mapping circuit to convert an input data word into a

converted data word based on both data bits and mask bits within the input data word, as recited in claim 28. In view of this clear distinction, neither independent claim 28, nor dependent claims 34-35, are anticipated by Nataraj.

Claim 62 recites, in part,

> converting the input data word, based on both data bits and mask bits therein, into a converted data word having a first pattern of constituent bits if the control signal is in a first state;
> converting the input data word, based on both the data bits and mask bits, into a converted data word having a second pattern of constituent bits if the control signal is in a second state;

As discussed above, Nataraj teaches receiving and decoding the prefix length value to generate a corresponding mask word, but does not teach converting the input data word, based on both data bits and mask bits therein, into a converted data, as recited in the above elements of claim 62. In view of this clear distinction, applicant submits that claim 62 is not anticipated by Nataraj.

Allowable Subject Matter

Claims 29-33 and 63-67 have been objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form, including all of the limitations of their respective base claims, and any intervening claims. In view of the above remarks, applicant submits that claims 29-33 and 63-67 are in condition for allowance. Accordingly, applicant has not amended these claims.

Conclusion

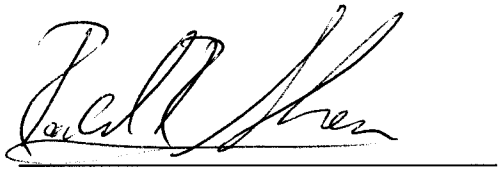
Applicant submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

A petition for a two (2) month extension of time is enclosed herewith.

Authorization is hereby given to charge deposit account 50-1914 for any fee deficiency associated with this Response.

Respectfully submitted
SHEMWELL MAHAMEDI LLP

Dated: June 6, 2006

By: 

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